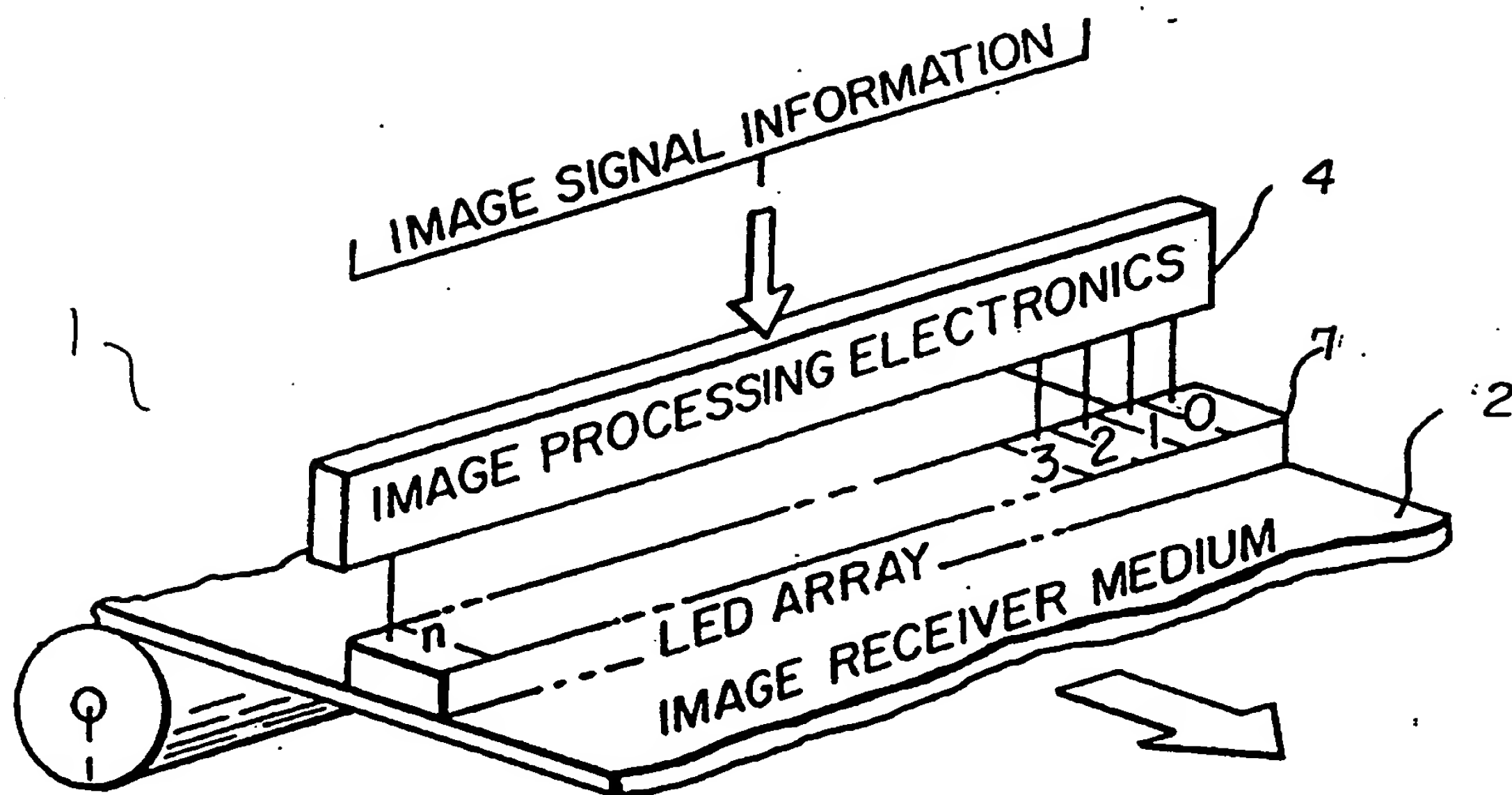


09870305-053004



**FIG. 1**  
**PRIOR ART**

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"FOF50" 50E07850

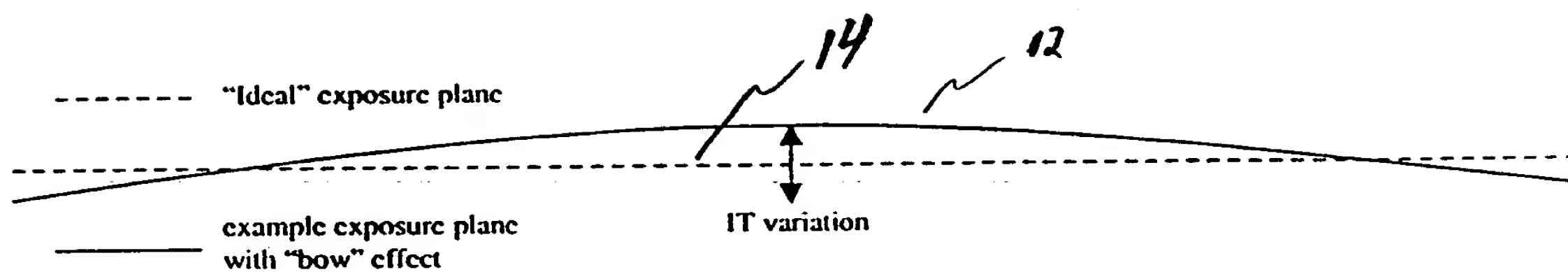


Figure 2a

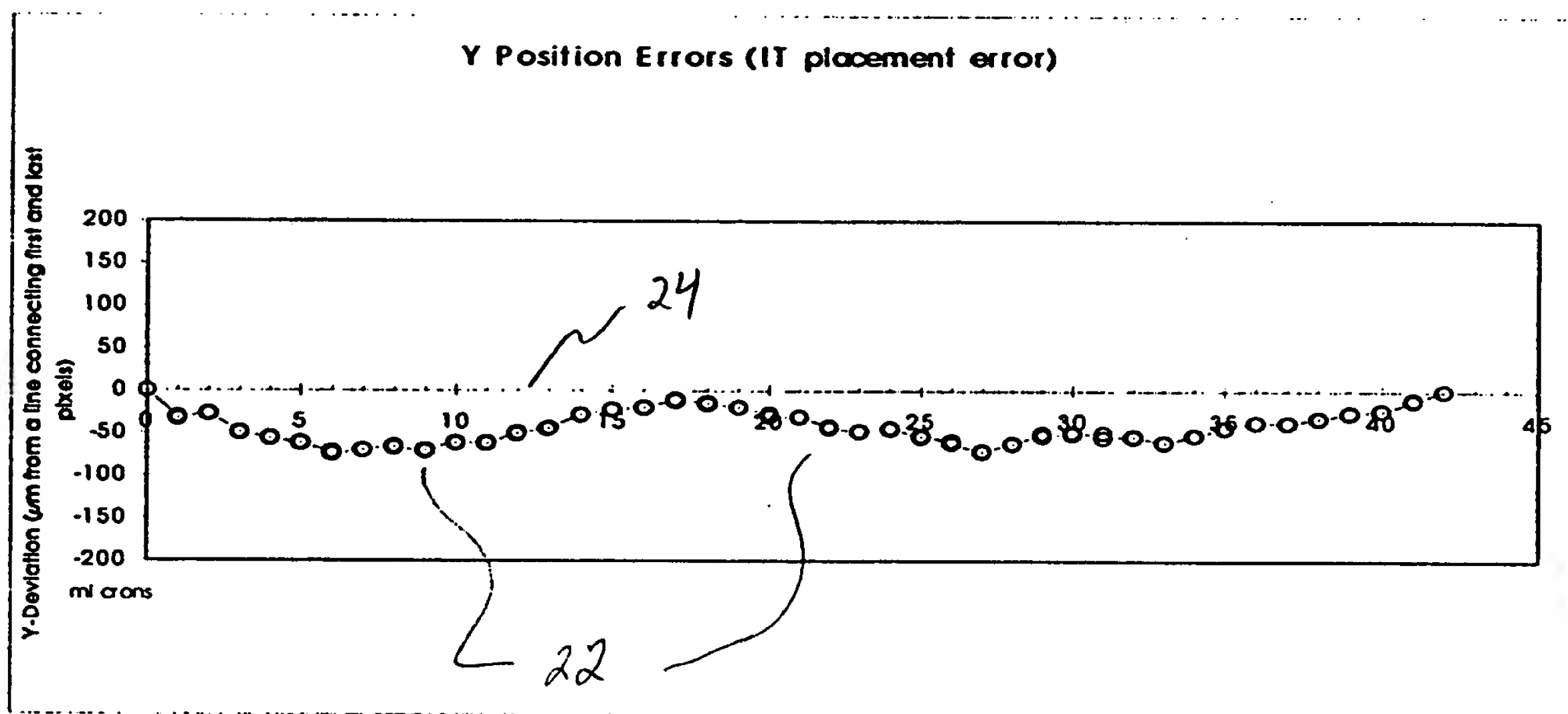


Figure 2b

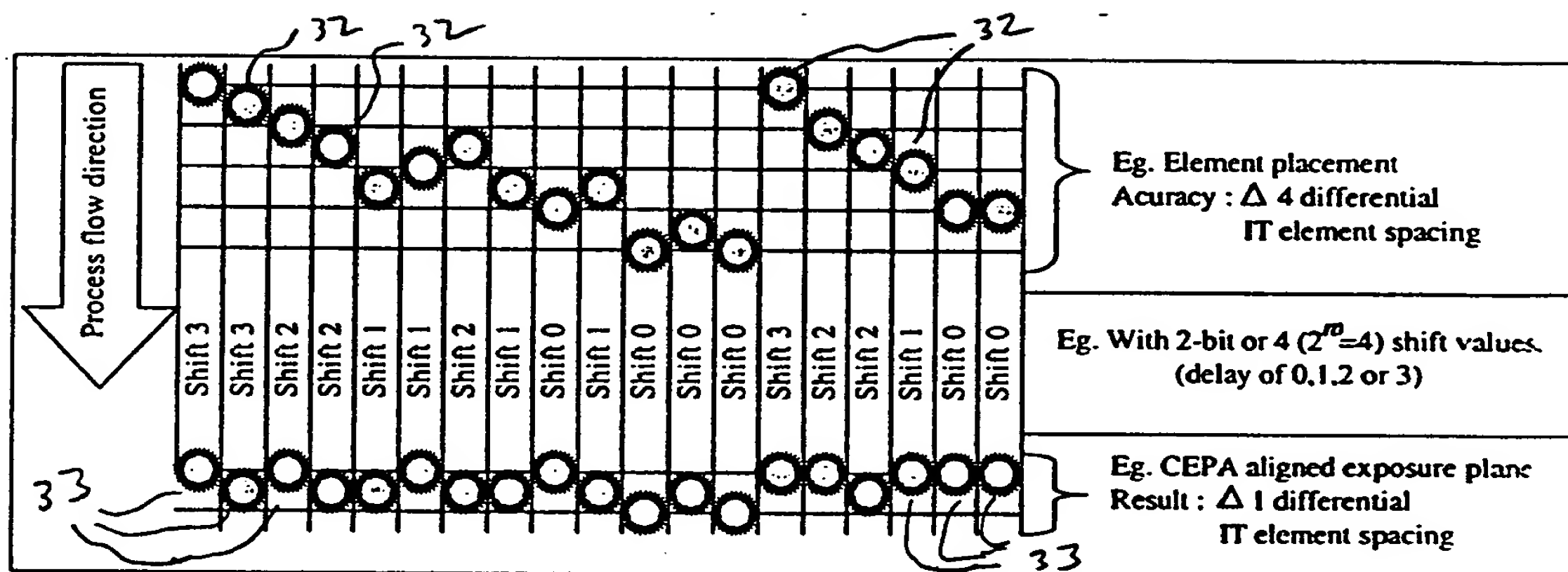


Figure 3 CEPA alignment example

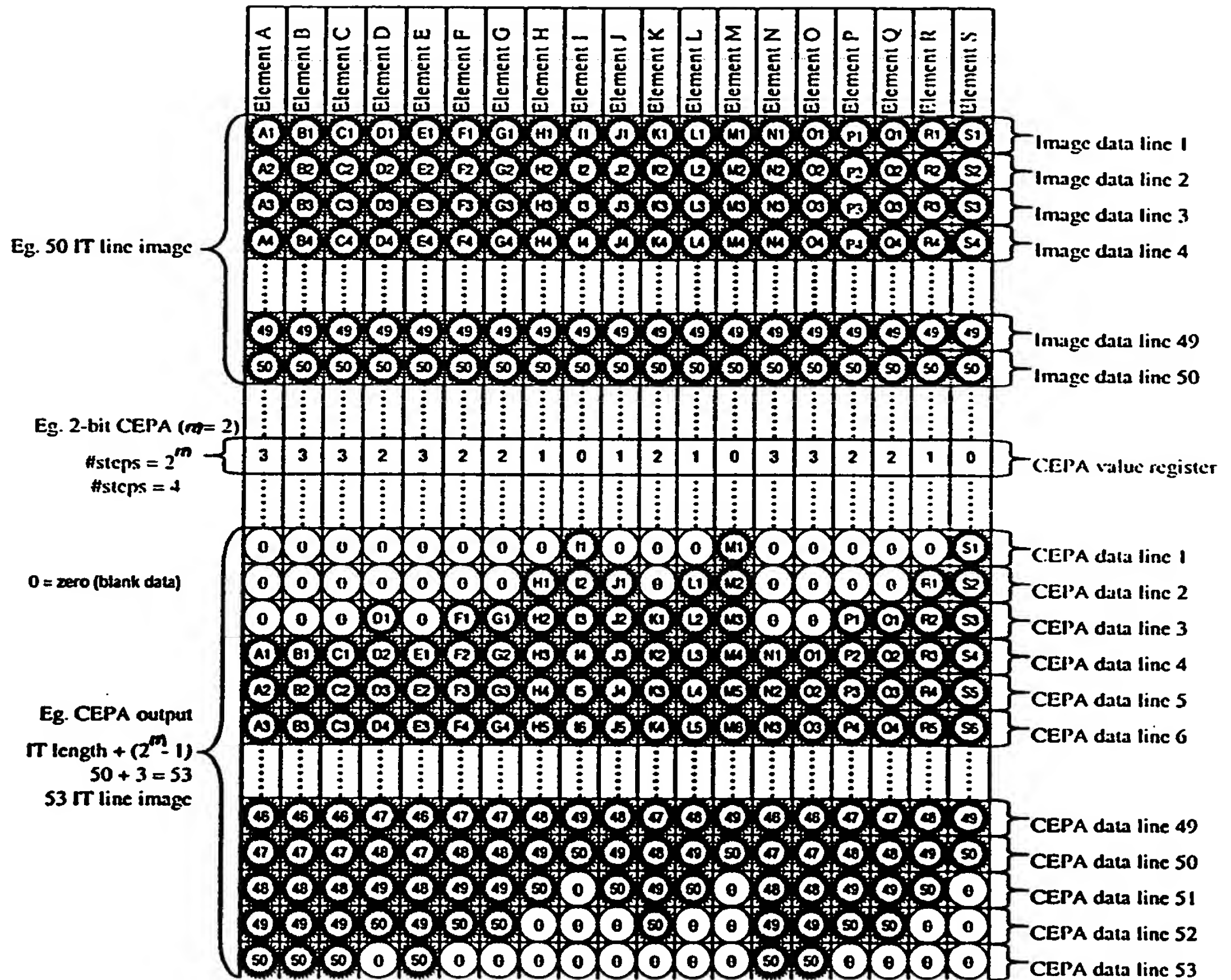


Figure 4 - CEPA data flow diagram

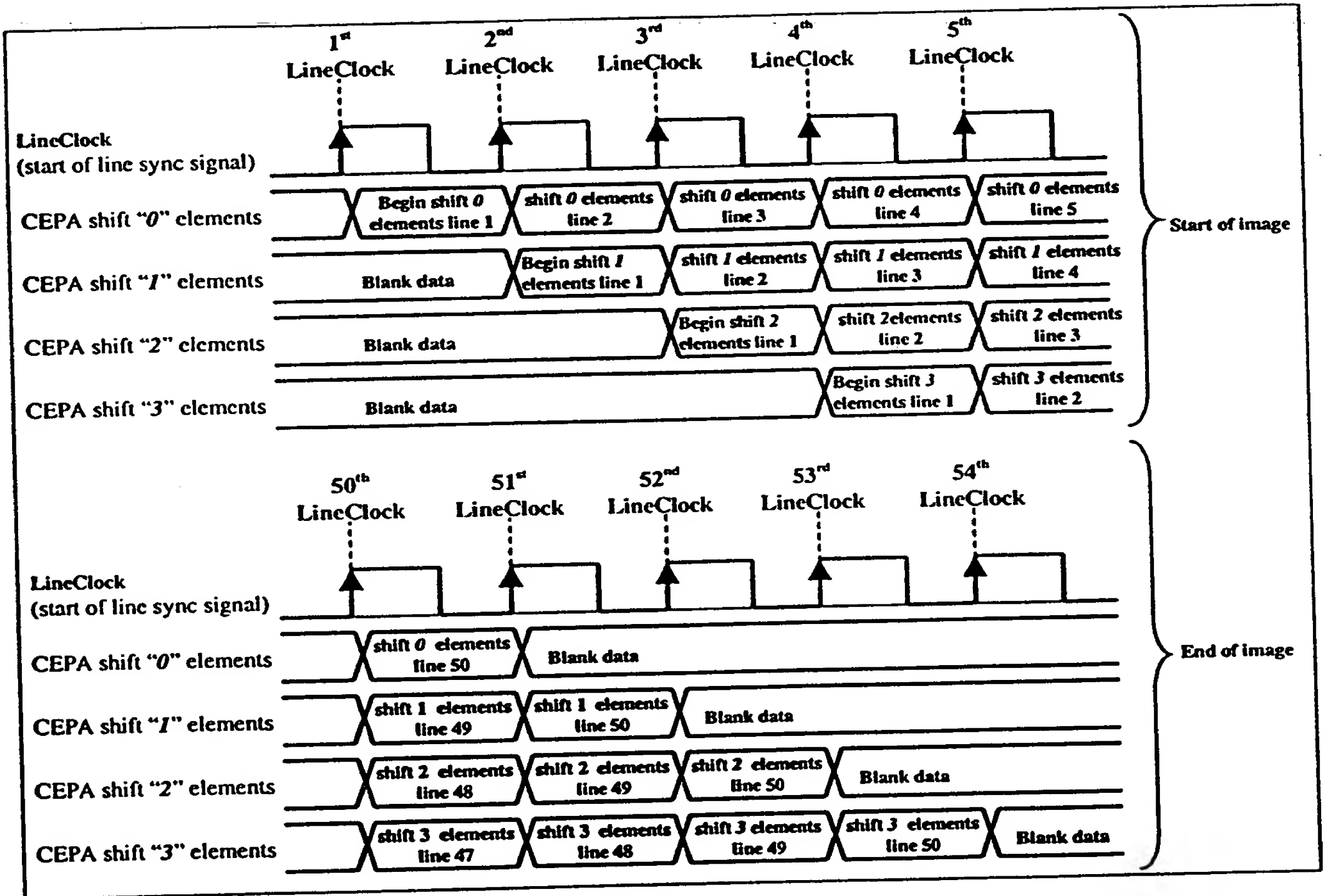


Figure 5 CEPA timing diagram (e.g. 50 IT line image)

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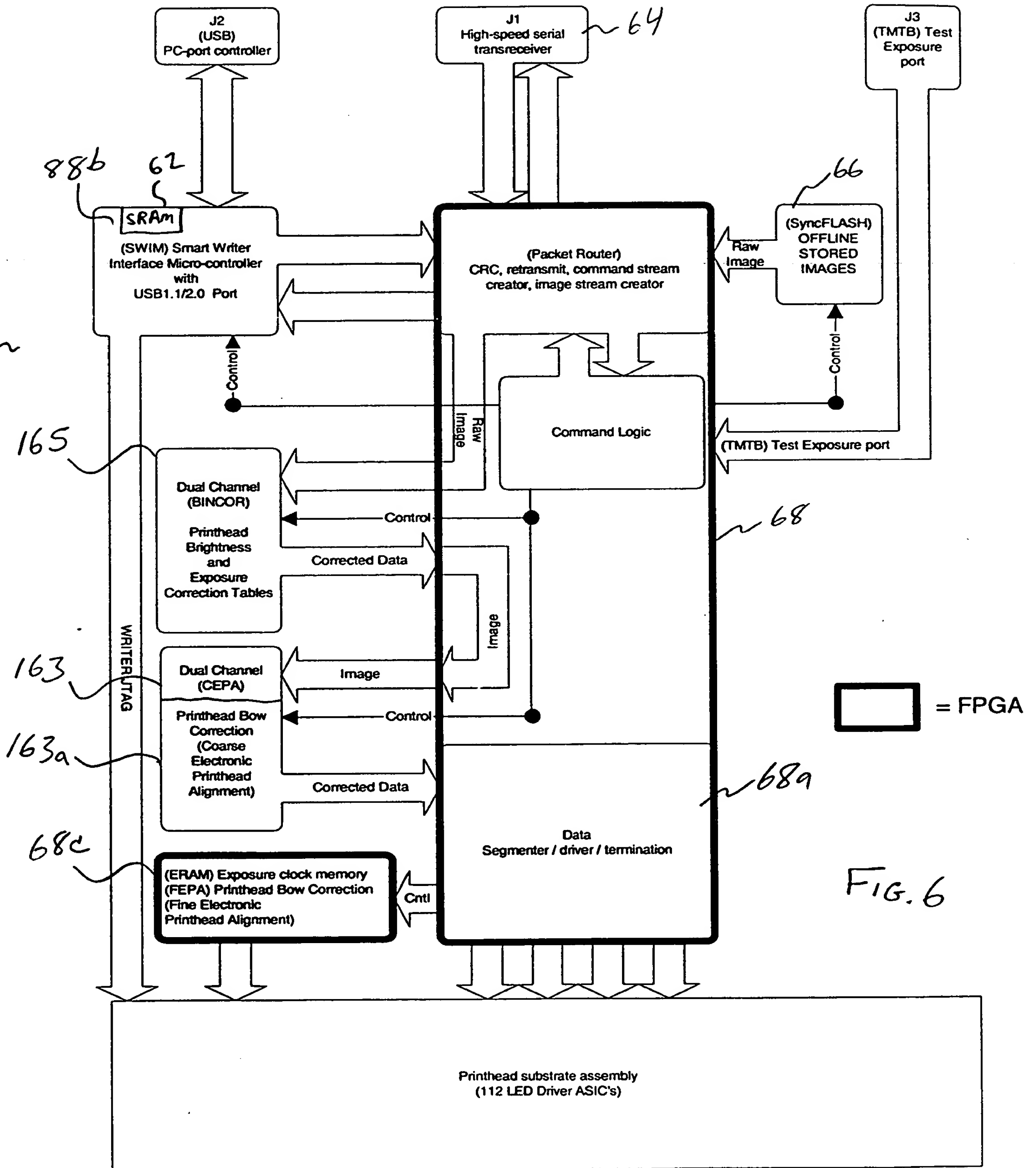


FIG. 6

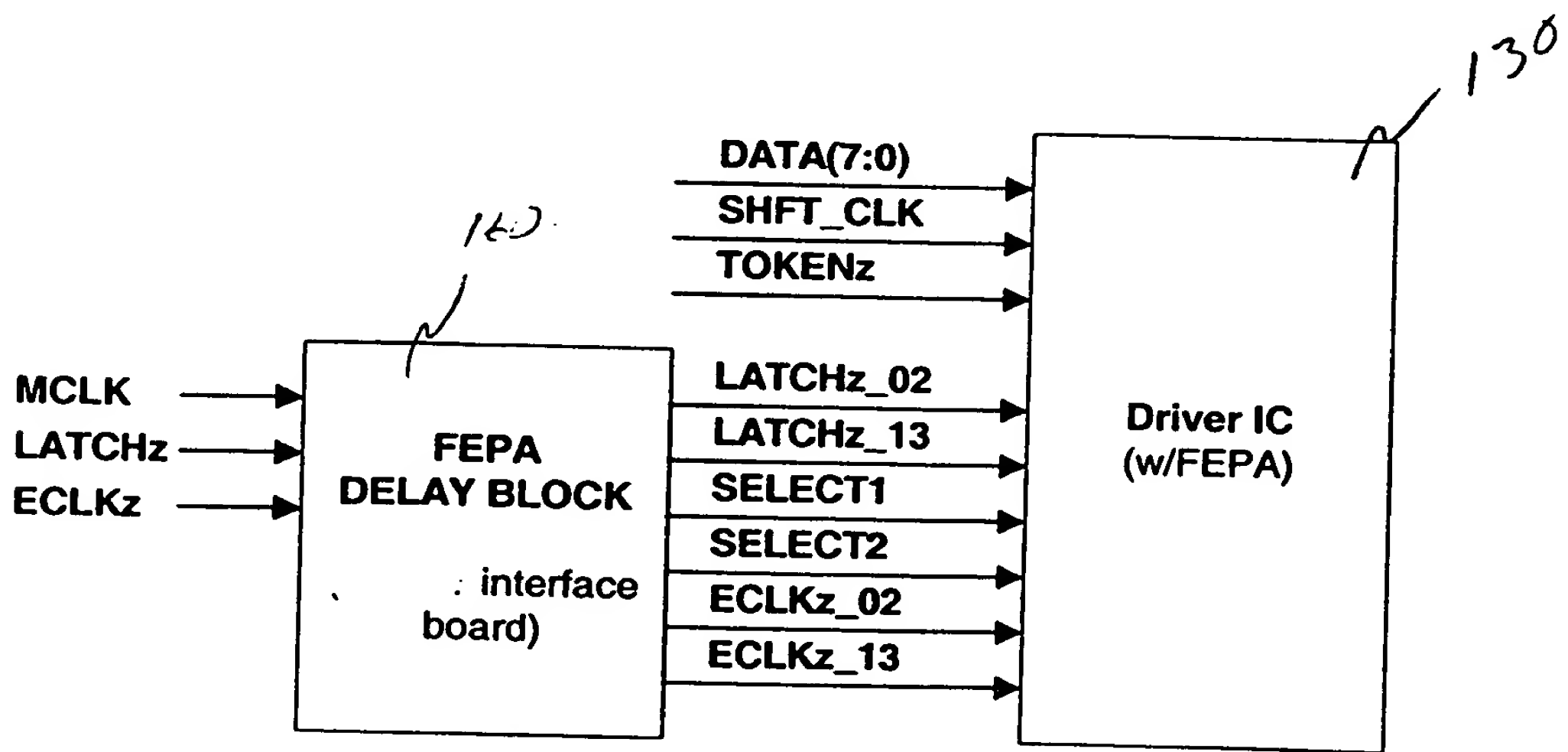
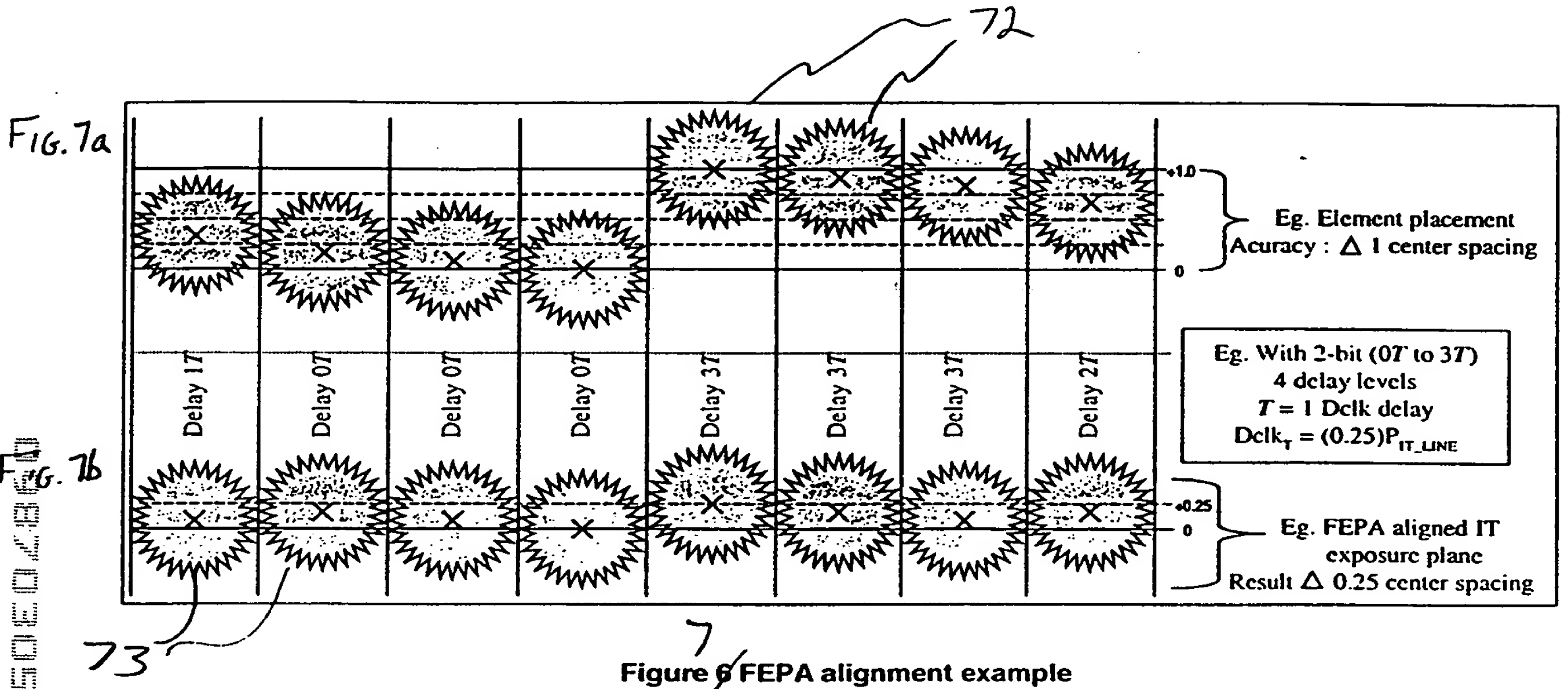


FIG. 8a FEPA BLOCK DIAGRAM

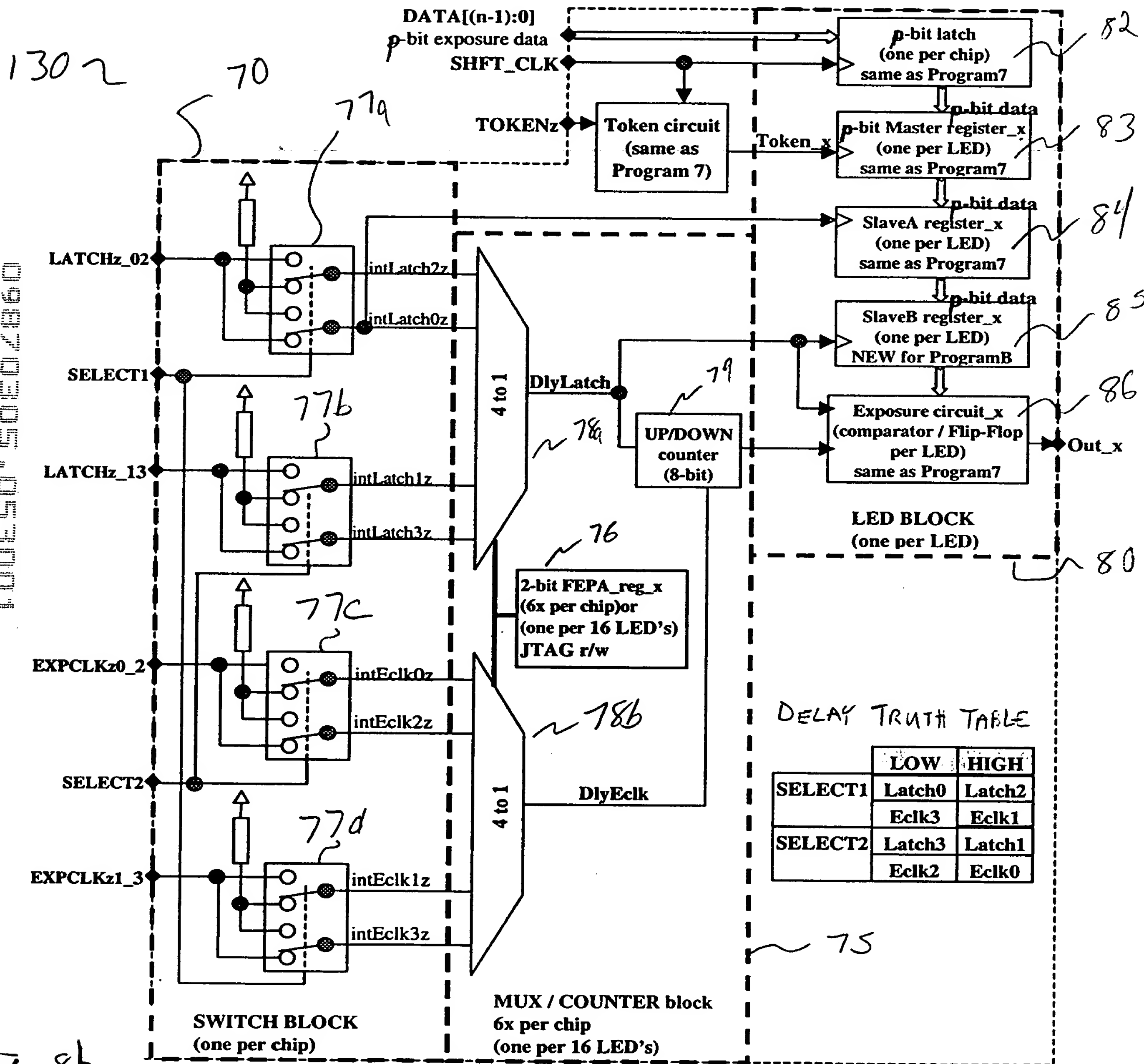


Fig 8b



130 ~

163

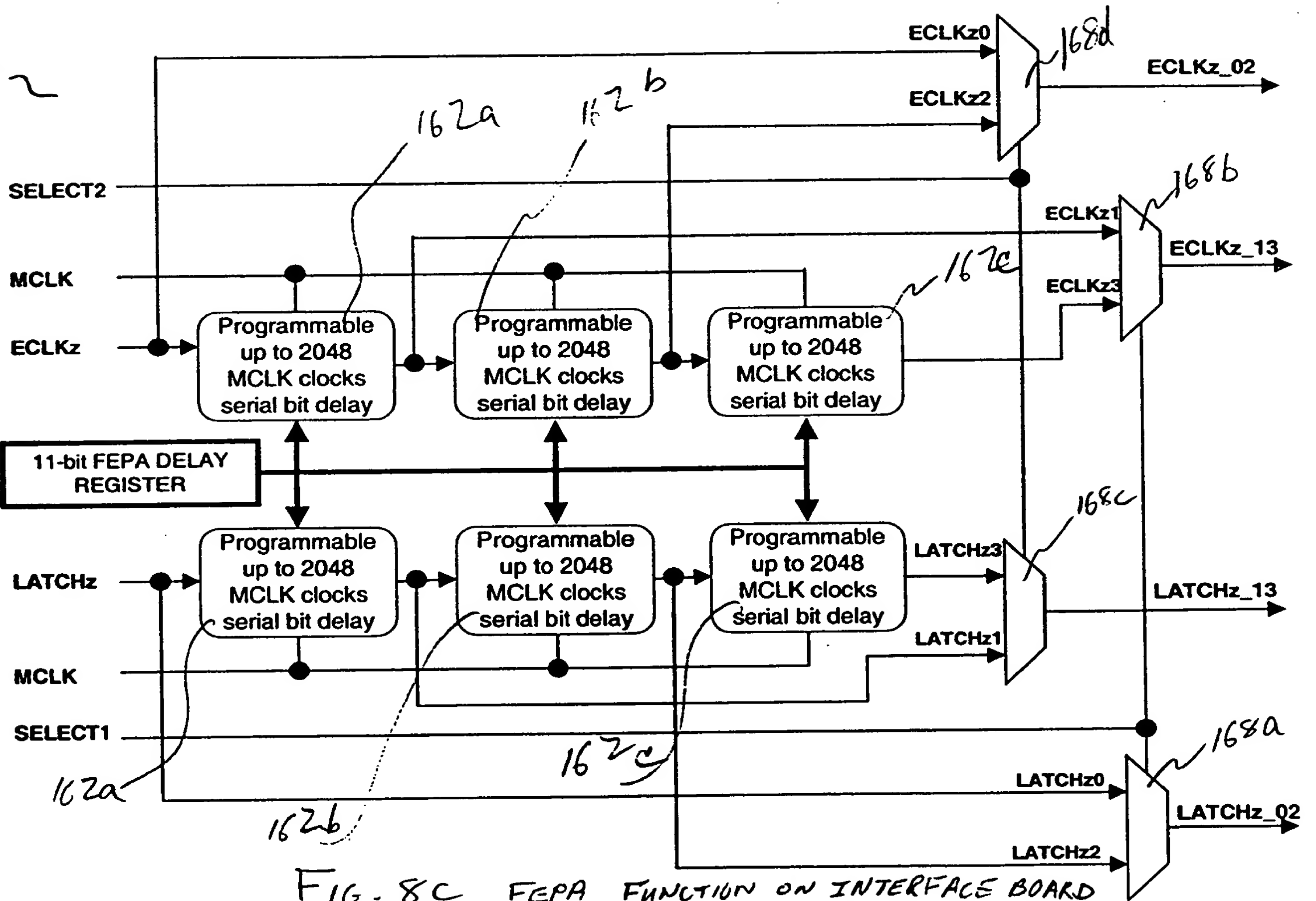


FIG. 8C FEPA FUNCTION ON INTERFACE BOARD

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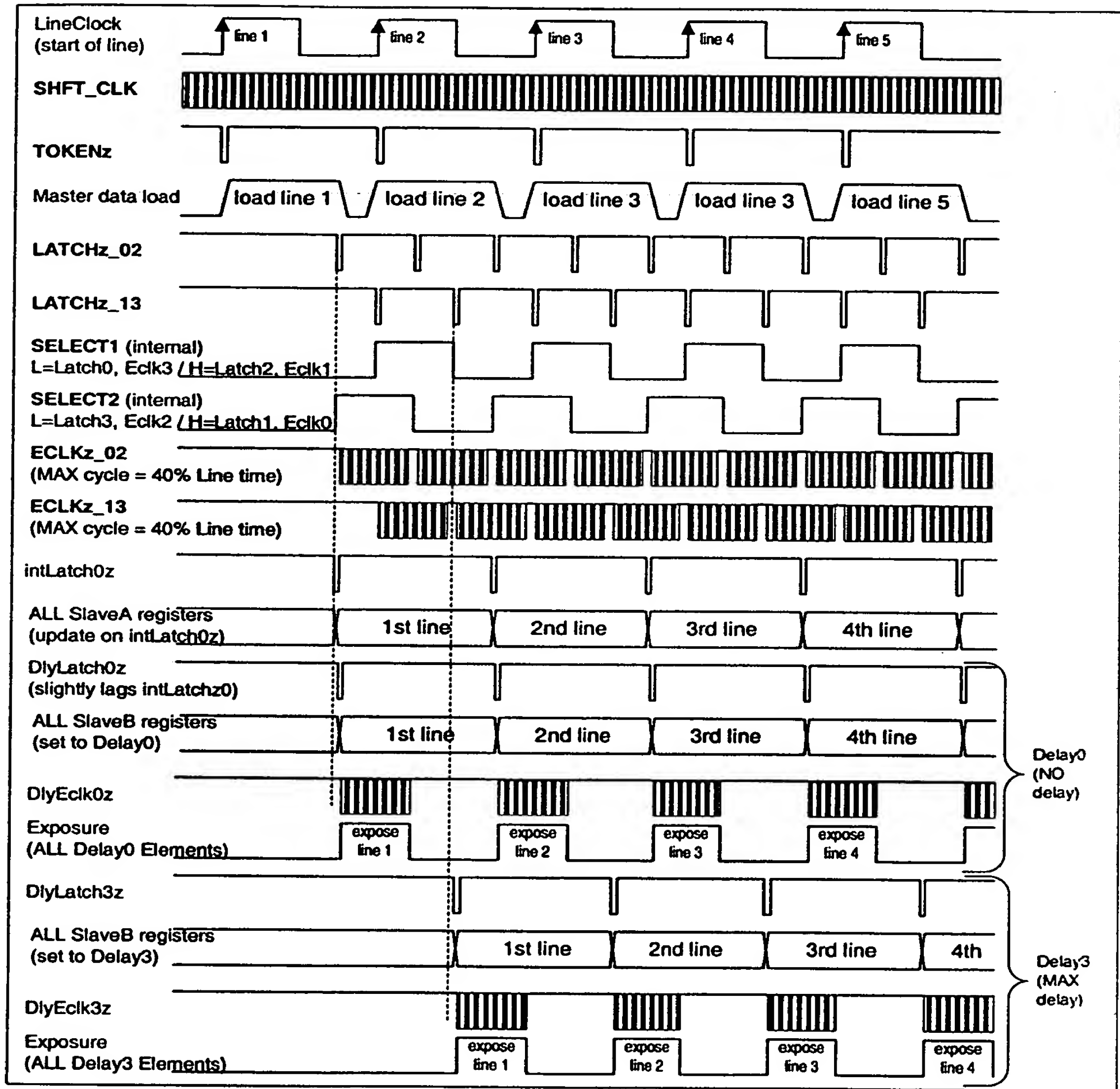


Fig 8d

TOP SECRET 05304

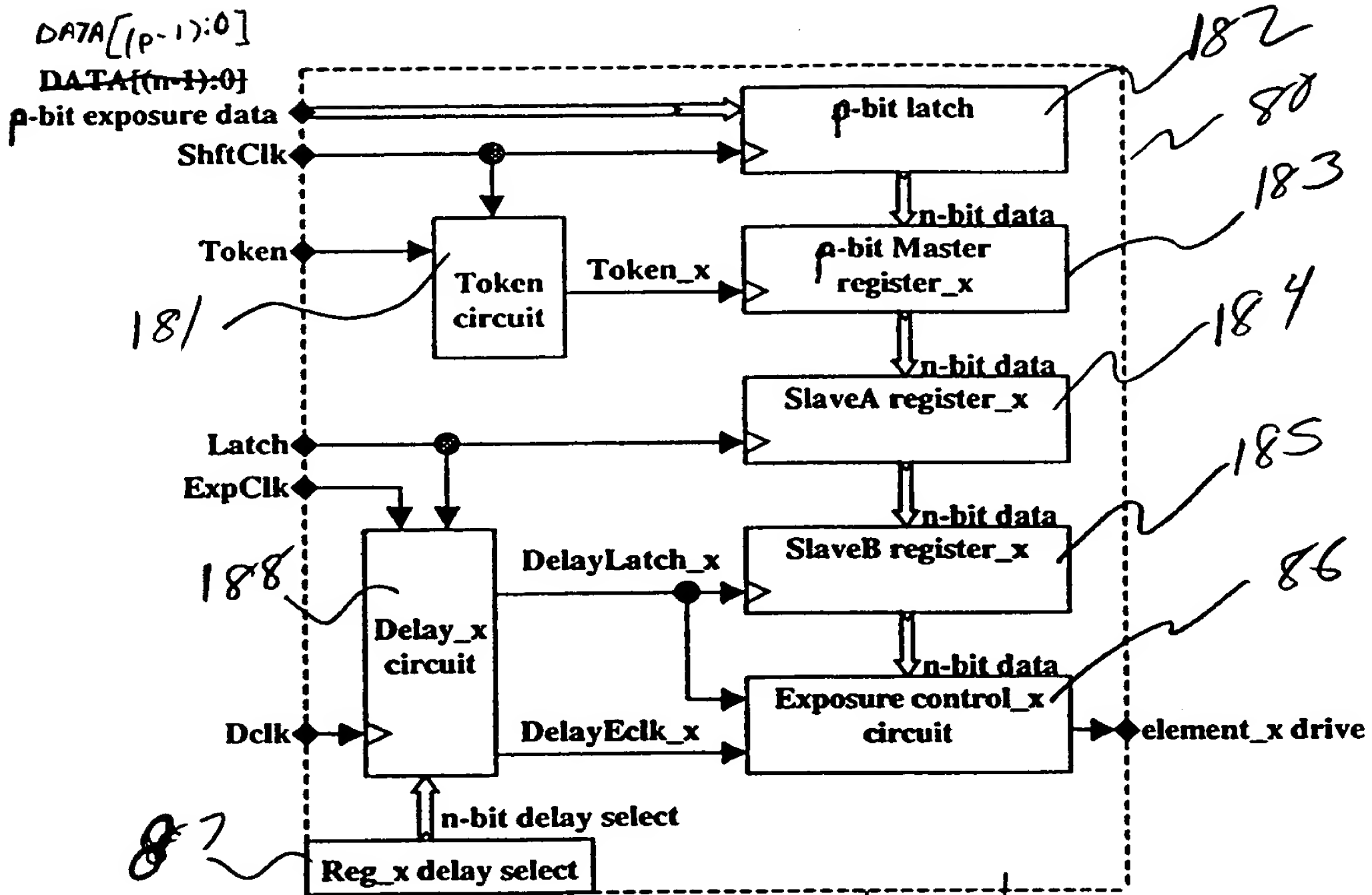


FIG. 9A FEPA DIAGRAM for Second Preferred Embodiment

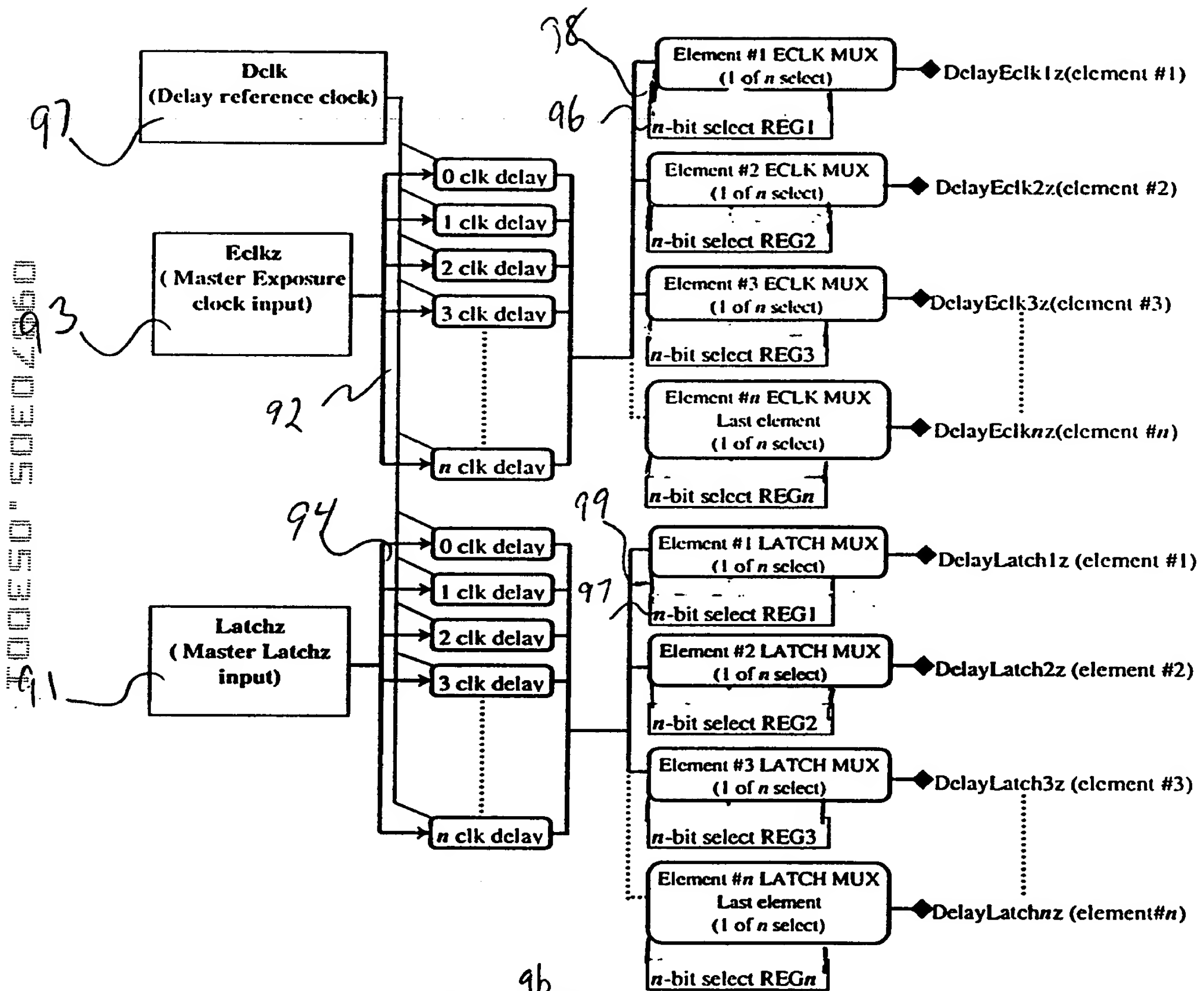
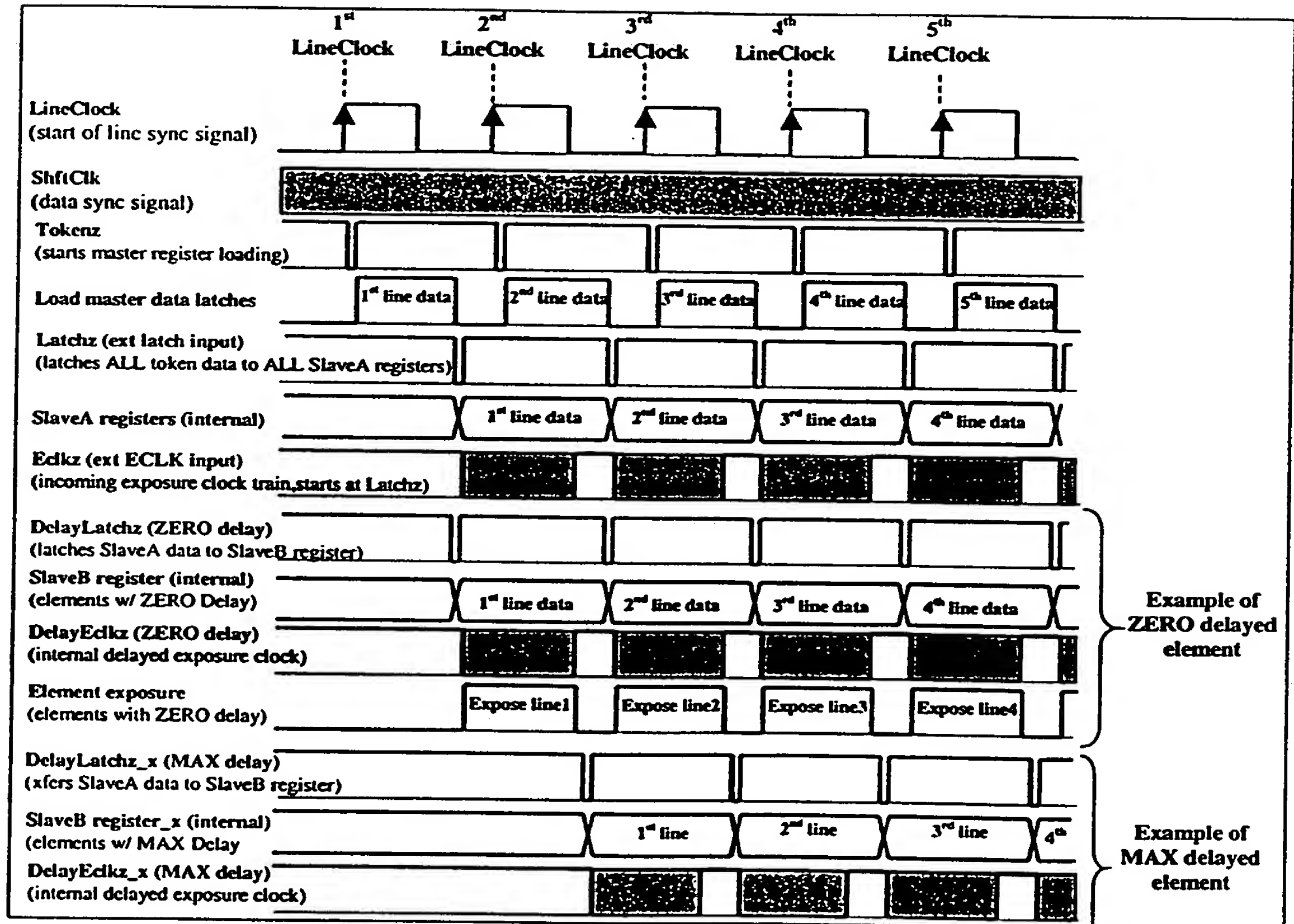


Figure 9b FEPA delay block diagram

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10  
Figure 9 FEPA signal timing diagram

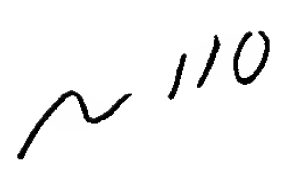
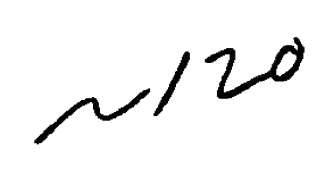
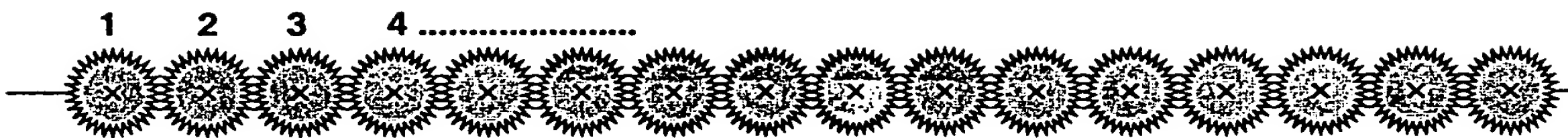


FIG. 12



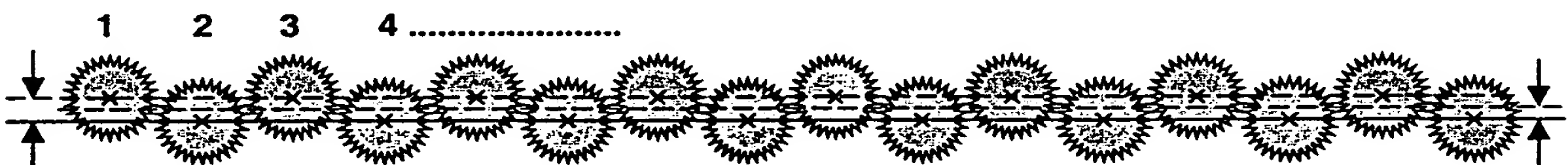
### FEPA DELAY SELECT CIRCUIT (ONE PER LED)

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Fig 13a



Odd and even shifted same

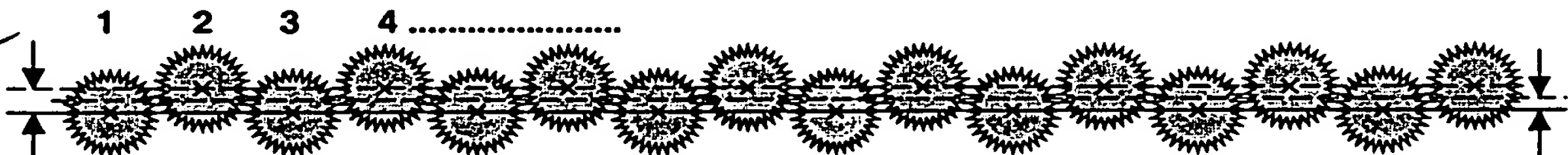
Fig 13b



Odd's only shifted +1/4 delta producing +1/8 average shift appearance

+1/8

Fig 13c



Even's only shifted +1/4 producing +1/8 average average shift appearance

+1/8

